REMARKS

This responds to the Office Action mailed on June 4, 2007.

Claims 1, 3, 5-11, 14-21, 23, 25-32, 34-38 are amended, claim 33 is canceled, and no claims are added; as a result, claims 1-32 and 34-38 are now pending in this application.

Information Disclosure Statement

The Examiner has objected to Applicant's Information Disclosure Statement. Specifically, the Examiner requested identification of all independent claim limitations that are known to exist in the Background art and IDS documentation filed 06/03/2005, 2/21/2006 and 08/17/2006.

Applicant respectfully states that the documents identified in the above Information Disclosure Statement are the references that were previously cited in the area of Applicant's invention. Applicant did not review the references in detail and thus cannot offer an opinion as to the relevance of particular references or particular parts thereof to the patentability of Applicant's invention.

§102 Rejection of the Claims

Claims 1, 2, 4, 5, 21, 22, 24, 25, 31, 32, 34 and 36 were rejected under 35 U.S.C. § 102(b) for anticipation by Bowles (US 5,796,980).

Applicant's invention as claimed in claims 1, 21, 31 and 34 pertains to a method and apparatus for decoupling write addresses from their corresponding write data in a store to a shared memory in a multiprocessor computer system. Specifically, Applicant teaches, and claims in claims 1, 21, 31 and 34, writing a write request address to a shared memory separate from its associated write data.

By separating the process of writing the data from the process of writing the address associated with the memory location where the date will be stored, a processor under Applicant's approach does not have to wait for write data to be produced before issuing a write request to a memory shared among a plurality of processors. Instead, the processor can start transferring the write request address independently of the write data as soon as the write request address

becomes available. The processor can transfer the write data later and pair it to the write request address stored in the shared memory.

For that purpose, Applicant teaches and claims, for example, in claim 1, noting the write request address in the shared memory; comparing, in the shared memory, addresses in subsequent load and store requests to the write request address; matching, within the shared memory, the write request address to its corresponding write data.

Although Bowles describes a method to reduce cache snooping overhead in a multilevel cache system, it does not teach or suggest decoupling the write request address from its corresponding write data as taught by Applicant and claimed in claims 1, 21, 31 and 34. For example, Applicant is unable to find portions in Bowles showing "noting the write request address in the shared memory" as claimed in claim 1.

Col. 1, lines 50-60 in Bowles cited by the Examiner merely describes general operations of 'hit' and 'miss' in a cache memory associated with a processor. Unlike the Examiner's assertion, however, the cited portion does not teach or suggest "comparing, in the shared memory, addresses in subsequent load and store requests to the write request address" as taught by Applicant and claimed in claim 1.

Furthermore, the Examiner also states that col. 5, lines 50-55 in Bowles teaches "matching, within the shared memory, the write request address to the write data" as claimed by Applicant in claim 1. Applicant respectfully disagrees. The cited portion states:

> (col. 5, line 50-58) The shared level 2 cache 30 contains data 30-1, tag or memory address of the data 30-2, and status of that data 30-3. In addition, the shared level 2 cache 30 contains an inclusion field array 30-4. The inclusion field array 30-4 contains separate indications identifying whether the tag-address of the data corresponding to the inclusion field also resides in any of the level 1 caches 20, 25 connected to the shared level 2 cache 30, and whether that data has been modified or not by the respective bus masters 10, 15.

As quoted above, the cited portion simply describes the data structure in the cache memory. There is no separation of write date and write address in sending them to the shared memory, and no subsequent matching of the data when it arrives to the previously sent write address in the shared memory. Instead, there is the matching of address to other addresses as is common in cache memory. This, therefore, teaches away from the matching process in the shared memory as taught by Applicant and claimed in claim 1. Similar arguments can be applied to other independent claims 21, 31 and 34. Claim 31 has been amended to emphasize these differences.

For these reasons, Bowles does not teach or suggest the method and apparatus for decoupling a write address from write data in a store to a shared memory in a multiprocessor computer system as taught by Applicant and claimed in claims 1, 21, 31 and 34. Reconsideration is respectfully requested.

With regard to claim 2 and 22, claims 2 and 22 are patentable as dependent on a patentable base claim. In addition, Bowles does not teach or suggest using a store address buffer in a shared memory or writing a write address in the store address buffer as taught by Applicant and claimed in claims 2 and 22. Fig. 2, Ref. 30-2 in Bowles is an address-array in a cache and not in a shared memory. Instead, as shown in Fig. 1 in Bowles, main memory is a separate entity from the level 1 or level 2 cache.

Fig. 5, block 626 in Bowles describes servicing a memory write access request if the level 2 cache is a "write-through" cache and there is a "hit" in the shared level 2 cache (see col. 11, lines 26-28 in Bowles). In that case, the level 2 cache will write the data to the cache memory and set a "modified" bit associated with that address. The portion does not, however, teach or suggest noting the write address in the store address buffer in the shared memory or subsequently matching write data to its associated write address in the shared memory as taught by Applicant and claimed in claims 2 and 22. Applicant is unable to find such teachings in Bowles. Reconsideration is respectfully requested.

With regard to claims 4 and 24, claims 4 and 24 are patentable as dependent on a patentable base claim. In addition, Bowles does not teach or suggest using a cache in a shared memory for noting a write address and for stalling subsequent load and store requests or subsequently matching write data to its associated write address in the shared memory as taught by Applicant and claimed in claims 4 and 24. Fig. 1, Ref. 30 and col. 1, lines 57-58 in Bowles describe the general hit and miss operations in a cache and not in a shared memory as noted in the discussion of claims 2 and 22. Applicant is unable to find such teachings in Bowles. Reconsideration is respectfully requested.

With regard to claims 5 and 25, claims 5 and 25 are patentable as dependent on a patentable base claim. In addition, Bowles does not teach or suggest using a bit vector in a shared memory for noting the write request address and for stalling subsequent load and store requests or subsequently matching write data to its associated write address in the shared

memory as taught by Applicant and claimed in claims 5 and 25. Col. 4, lines 1-2 in Bowles describe a status field in a cache and not in shared memory as noted in the discussion of claim 2 and 22. Applicant is unable to find such teachings in Bowles. Reconsideration is respectfully requested.

With regard to claims 32 and 36, claims 32 and 36 are patentable as dependent on a patentable base claim.

§103 Rejection of the Claims

Claims 3, 6-10, 23, 26-30, 33, 35, 37 and 38 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bowles in view of Frink et al. (US 5,530,933).

Bowles is discussed above.

Frink describes maintaining cache coherency in a multiprocessor system by checking the coherency in the order of the transactions being issued on the bus. Specifically, Frink describes reordering a cache write to be processed before an earlier cache coherent read transaction if the cache write conflicts with the coherent read transaction.

Neither Bowles nor Frink, however, alone or in combination, teach or suggest decoupling a write address from its associated write data or subsequently matching the write request address to its corresponding write data in the shared memory as taught by Applicant and claimed in claim 38. Claim 38 has been amended to further emphasize these differences. Reconsideration is respectfully requested.

With regard to claims 9, 29 and 37, claims 9, 29 and 37 are patentable as dependent on a patentable base claim. In addition, neither Bowles nor Frink teach or suggest enforcing memory ordering, in a shared memory, in subsequent read and write requests to their associated write requests or subsequently matching write data with its associated write address in the shared memory as taught by Applicant and claimed in claims 9, 29 and 37. Reconsideration is respectfully requested.

With regard to claims 3, 6-8, 10, 23, 26-28, 30, 33 and 35, claims 3, 6-8, 10, 23, 26-28, 30, 33 and 35 are patentable as dependent on a patentable base claim.

Allowable Subject Matter

Claims 11-20 have been allowed.

RESERVATION OF RIGHTS

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date October 11, 2007

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 11 day of October, 2007.

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